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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,847	05/11/2001	Shinji Ohuchi	OKI.234	5682

7590 06/30/2004

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/852,847	OHUCHI ET AL.	
	Examin r	Art Unit	
	Monica Lewis	2822	

-- Th MAILING DATE of this communication appears on the cov r sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-29* is/are pending in the application.

4a) Of the above claim(s) *9-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed April 5, 2004.

Response to Arguments

2. Applicant's arguments with respect to claims 18-29 have been considered but are moot in view of the new ground(s) of rejection.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21 and 22 recite the limitation "sealed confronting surfaces." There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

6. Claim 27 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 18-20 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Drawings in view of Eide (U.S. Patent No. 5,313,096).

In regards to claim 18, Applicant's Prior Art Drawings disclose the following:

a) a semiconductor element (601) having a circuit forming surface and a parallel confronting surface (For Example: See Figure 21);

b) a wiring (604) disposed on said circuit forming surface (For Example: See Figures 21 and 22);

c) a sealed bump electrode (602) connected to said wiring (For Example: See Figure 21 and 22);

d) sealed bump electrode having an exposed surface (For Example: See Figure 21); and

e) an outer electrode (603) disposed on said exposed surface of said bump electrode (For Example: See Figure 21).

In regards to claim 18, Applicant's Prior Art Drawings fail to disclose the following:

a) sealed parallel confronting surface.

However, Eide discloses a sealed confronting surface (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a sealed

confronting surface as disclosed in Eide because it aids in providing high chip density (For Example: See Column 8 Lines 34 and 35).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

b) outer electrode contacting said wiring on said side surface of said semiconductor element.

However, Eide discloses an outer electrode (60) contacting wiring on said side surface of the semiconductor element (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include an outer electrode contacting wiring on said side surface as disclosed in Eide because it aids in coupling chip packages in parallel (For Example: See Column 4 Lines 27 and 28).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 19, Applicant's Prior Art Drawings disclose the following:

a) a plurality of electrodes on said circuit forming surface (For Example: See Figure 21).

In regards to claim 20, Applicant's Prior Art Drawings fails to disclose the following:

a) wiring on a side surface has an end that is sealed.

However, Eide discloses wiring on said side surface that is sealed (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the

invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include wiring on said side surface that is sealed as disclosed in Eide because it aids in coupling chip packages in parallel (For Example: See Column 4 Lines 27 and 28).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 22, Applicant's Prior Art Drawings fail to disclose the following:

a) sealed confronting surface is entirely sealed.

However, Eidi discloses a sealed confronting surface (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a sealed confronting surface as disclosed in Eidi because it aids in providing high chip density (For Example: See Column 8 Lines 34 and 35).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 23, Applicant's Prior Art Drawings fail to disclose the following:

a) a semiconductor device mounted on a second semiconductor device.

However, Eide discloses two semiconductor devices mounted on each other (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art

Drawings to include two semiconductor devices mounted on each other as disclosed in Eide because it aids in providing high chip density (For Example: See Column 8 Lines 34 and 35).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 24, Applicant's Prior Art Drawings fail to disclose the following:

a) another semiconductor device has electrodes that are connected to said wiring of the semiconductor device.

However, Eide discloses two semiconductor devices have electrodes that are connected to the wiring (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices that are connected as disclosed in Eide because it aids in coupling chip packages in parallel (For Example: See Column 4 Lines 27 and 28).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 25, Applicant's Prior Art Drawings fail to disclose the following:

a) semiconductor device is mounted on another semiconductor device with said confronting surface as a contacting surface, and said another semiconductor device has electrodes that are connected to said wiring and to at least one of said plurality of electrodes.

However, Eide discloses two semiconductor devices mounted on each other with said confronting surface as a contacting surface and another semiconductor device has electrodes (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the

time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include two semiconductor devices mounted with said confronting surface as a contacting surface and another semiconductor device has electrodes as disclosed in Eide because it aids in providing high chip density (For Example: See Column 8 Lines 34 and 35).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 26, Applicant's Prior Art Drawings fail to disclose the following:

a) another semiconductor device is disposed over a plurality of other semiconductor devices.

However, Eide discloses a semiconductor device disposed over other devices (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a semiconductor device disposed over other devices as disclosed in Eide because it aids in providing high chip density (For Example: See Column 8 Lines 34 and 35).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 27, Applicant's Prior Art Drawings fail to disclose the following:

a) a part of said outer electrode is disposed on said wiring.

However, Eide discloses an outer electrode on said wiring (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include an outer

electrode disposed on said wiring as disclosed in Eide because it aids in coupling chip packages in parallel (For Example: See Column 4 Lines 27 and 28).

Additionally, since Applicant's Prior Art Drawings and Eide are both from the same field of endeavor, the purpose disclosed by Eide would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

9. Claims 21, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Drawings in view of Eide et al. (U.S. Patent No. 5,313,096) and Mori (U.S. Patent No. 5,903,049).

In regards to claim 21, Applicant's Prior Art Drawings disclose the following:

a) sealed bump electrode is resin sealed (For Example: See Specification Page 2 Lines 1 and 2).

In regards to claim 21, Applicant's Prior Art Drawings fail to disclose the following:

a) surface is resin sealed.

However, Mori discloses the use of resin (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include the use of resin as disclosed in Mori because it aids in protecting the elements from the surrounding environment (For Example: See Column 2 Lines 57 and 58).

Additionally, since Applicant's Prior Art Drawings and Mori are both from the same field of endeavor, the purpose disclosed by Mori would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 28, Applicant's Prior Art Drawings disclose the following:

a) said circuit forming surface is sealed (For Example: See Figure 21).

In regards to claim 29, Applicant's Prior Art Drawings discloses the following:

a) circuit forming surface is resin sealed (For Example: See Figure 21).

In regards to claim 29, Applicant's Prior Art Drawings fail to disclose the following:

a) parallel confronting surface is sealed.

However, Mori discloses the use of resin (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include the use of resin as disclosed in Mori because it aids in protecting the elements from the surrounding environment (For Example: See Column 2 Lines 57 and 58).

Additionally, since Applicant's Prior Art Drawings and Mori are both from the same field of endeavor, the purpose disclosed by Mori would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

Conclusion

10. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Chung (U.S. Patent No. 6,376,769) discloses a high density electronic package; b) Akram et al. (U.S. Patent No. 6,025,365) discloses an integrated circuit package; c) Normington (U.S. Patent No. 5,281,852) discloses semiconductor device including stacked die; d) Kimoto et al. (U.S. Patent No. 6,576,971) discloses a chip type electronic part; e) Horie et al. (U.S. Patent No. 5,508,562) discloses an outer electrode structure; f) Pan (U.S. Patent

No. 6,501,663) discloses an interconnect system; g) Hashimoto (U.S. Patent No. 6,486,544) discloses a semiconductor device; and h) Jairazbhoy et al. (U.S. Patent No. 6,303,872) discloses solder joints.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

June 18, 2004

Mary Wilczewski
Primary Examiner